Lab 2 Report: Group 8

Using Quartus Prime and the DE2 Board

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Abstract –

Lab 2 was intended to get the team accustomed to using ModelSim and programming with VHDL files. The team designed logic gates, then compiled them to be used in ModelSim for reading timing graphs and understanding the output of our designed gates.

Introduction –

Lab 1 was about getting the team comfortable with using ModelSim and working with programming logic gates in VHDL files to later be compiled and used in other ways. The team imported an XOR gate to be read in ModelSim’s waveform graph and became accustomed to reading inputs and outputs from that type of figure. The team then created an AND gate by programming it into a VHDL file, and compiled it into a symbol file for use in a BDF project. After this, we again compiled it for review in ModelSim and interpreted the waveform graph.